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PATENT APPLICATION

ATTORNEY DOCKET NO. 10001197-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

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By:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): ☒ Utility ☐ Design
☐ original patent application,
☐ continuation-in-part application

JC917 U.S. PTO
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INVENTOR(S): David Brandon Miller et al

TITLE: Aligning An Optical Device System With An Optical Lens System

Enclosed are:

- ☒ The Declaration and Power of Attorney. ☒ signed ☐ unsigned or partially signed
☒ 5 sheets of drawings (one set) ☐ Associate Power of Attorney
☒ Form PTO-1449 ☒ Information Disclosure Statement and Form PTO-1449
☐ Priority document(s) ☐ (Other) (fee \$)

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ANY MULTIPLE DEPENDENT CLAIMS	0		\$270	\$ 0
BASIC FEE: Design \$320.00); Utility \$710.00				\$ 710
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Charge \$ 710 to Deposit Account 50-1078. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 50-1078 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 50-1078 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

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By Ann Marie Radcliffe
Typed Name: Ann Marie Radcliffe

Respectfully submitted,

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ALIGNING AN OPTICAL DEVICE SYSTEM WITH AN OPTICAL LENS SYSTEM

TECHNICAL FIELD

This invention relates to systems and methods for aligning an optical
5 device system with an optical lens system.

BACKGROUND

Many advanced communication systems transmit information through a plurality of parallel optical communication channels. The optical communication channels may be defined by a fiber optic ribbon interconnect (or fiber optic cable)
10 formed from a bundle of glass or plastic fibers, each of which is capable of transmitting data independently of the other fibers. Relative to metal wire interconnects, optical fibers have a much greater bandwidth, they are less susceptible to interference, and they are much thinner and lighter. Because of these advantageous physical and data transmission properties, efforts have been
15 made to integrate fiber optics into computer system designs. For example, in a local area network, fiber optics may be used to connect a plurality of local computers to centralized equipment, such as servers and printers. In this arrangement, each local computer has an optical transceiver for transmitting and receiving optical information. The optical transceiver may be mounted on a
20 printed circuit board that supports one or more integrated circuits. Typically, each computer includes several printed circuit boards that are plugged into the sockets of a common backplane. The backplane may be active (i.e., it includes logic circuitry for performing computing functions) or it may be passive (i.e., it does not contain any logic circuitry). An external network fiber optic cable may
25 be connected to the optical transceiver through a fiber optic connector that is coupled to the backplane.

Vertical cavity surface emitting lasers (VCSELs) are becoming an important element of fiber optic links in modern data communication. For example, VCSELs have replaced light-emitting diodes (LEDs) in all local area network (LAN)
30 applications for data rates of 1 Gigabits-per-second (Gb/s) or higher. The rapid increase in Internet traffic is creating communications bottlenecks in the back plane of computers and in the switches and routers that direct the data flow

throughout computer networks. Since these applications cover a relatively short distance (e.g., about 1-100 meters), it is more economical to use parallel links over multiple fibers rather than higher speed serial links over a single fiber. Of particular interest is an application with twelve channels operating at 2.5 Gb/s.

5 For short distance applications in which the cost of twelve-fiber ribbon interconnects is relatively low, this parallel solution is less expensive than a serial channel operating at the combined data rate of 30 Gb/s. Ribbon interconnects with four fibers, eight fibers and sixteen fibers operating at data rates of 1-10 Gb/s per channel and with aggregate throughputs in excess of 100 Gb/s are expected to
10 be developed within the next two years.

By design, a VCSEL emits laser light from the top surface of a light-emitting cavity with a relatively small beam divergence (e.g., on the order of 10°). These features allow VCSELs to be arranged in one-dimensional or two-dimensional arrays, tested in parallel, and easily incorporated into an optical transceiver
15 module and coupled to a fiber optic ribbon interconnect. Efforts have been made to simplify the problem of aligning the optical ports of an optical transceiver module with the fibers of a fiber optic ribbon interconnect. In one single-fiber alignment approach, the optoelectronic device is die and wire bonded to a transceiver package so that it may be biased to its normal operating condition.
20 The input end of the fiber is mechanically manipulated in front of the active region of the optoelectronic device until an optical coupling between the fiber and the optoelectronic device is achieved. After the optimal coupling has been achieved, the optoelectronic device is bonded in place. This process requires either human interaction or expensive equipment that automatically dithers the
25 fiber into the optimal position. This conventional alignment process becomes significantly more complicated when applied to the coupling of arrays of optical fibers with arrays of optoelectronic devices. Additional difficulties arise when an optical lens system must be aligned between the optoelectronic devices and the optical fibers.

30

SUMMARY

The invention features a scheme (systems and methods) for passively aligning one or more optical devices with a corresponding number of optical

lenses in an accurate and efficient manner. By this approach, the invention avoids the often labor-intensive and costly steps required by conventional active alignment techniques that attempt to align the optical devices to the optical fibers.

In one aspect, the invention features an optoelectronic device, comprising
5 an optical device system, an optical lens system and a plurality of solder bumps disposed therebetween. The optical device system includes an optical device substrate supporting one or more optical devices and a solderable metallization pattern having a spatial arrangement with respect to the one or more optical devices. The optical lens system includes one or more optical lenses and a device
10 bonding surface supporting a solderable metallization pattern having a spatial arrangement with respect to the one or more optical lenses. The solder bumps are disposed between the metallization patterns of the optical device system and the optical lens system. The plurality of solder bumps bond the optical device substrate to the device bonding surface with the one or more optical devices
15 aligned with the one or more optical lenses.

Embodiments in accordance with this aspect of the invention may include one or more of the following features.

The one or more optical lenses may be incorporated into the device bonding surface. Alternatively, the one or more optical lenses may be recessed
20 below the device bonding surface.

In some embodiments, the optical lens system includes an optical substrate incorporating the one or more lenses and the device bonding surface defines one face of a spacer substrate. The optical substrate may be bonded to the spacer substrate by a wafer bonding process or a flip-chip solder bonding process. The
25 thickness of the device bonding substrate preferably is selected based upon a representative focal distance between the one or more optical devices and the one or more optical lenses. The spacer substrate may be transparent or it may comprise one or more apertures through which light is transmitted between the one or more optical devices and the one or more optical lenses. An integrated
30 circuit may be formed on the spacer substrate and may be configured to drive the one or more optical devices. Alternatively, the integrated circuit may be bonded to the spacer substrate by a flip-chip solder bonding process.

connections. This feature reduces inductance and electromagnetic interference (EMI) emissions commonly associated with such wirebond connections.

Other features and advantages of the invention will become apparent from the following description, including the drawings and the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a diagrammatic side view of a vertical cavity surface emitting laser.

FIG. 2 is a diagrammatic side view of an optical device system aligned and bonded to an optical lenses system.

FIG. 3 is a diagrammatic side view of an optical device system aligned and bonded to an optical lens system having an optical element recessed below a device bonding surface.

FIG. 4A is a diagrammatic side view of an optical device system aligned and bonded to an optical lenses system formed from a spacer substrate that is bonded to an optical substrate by a wafer bonding process.

FIG. 4B is a diagrammatic side view of an optical device system aligned and bonded to an optical lenses system formed from a spacer substrate that is bonded to an optical substrate by a solder bump reflow process.

FIG. 5A is a diagrammatic side view of an optical device system including an array of optical devices aligned and bonded to an optical lens system formed from an optical substrate and a spacer substrate having a single aperture.

FIG. 5B is a diagrammatic side view of an optical device system including an array of optical devices aligned and bonded to an optical lens system formed from an optical substrate and a spacer substrate having a plurality of apertures.

FIG. 6A is a diagrammatic side view of an optical device system bonded to a spacer substrate with an integral integrated circuit.

FIG. 6B is a diagrammatic side view of an optical device system bonded to a spacer substrate to which an integrated circuit is bonded by a flip-chip solder bonding process.

FIG. 7A is a diagrammatic top view of an optical device array and a pair of staggered arrays of solderable bonding pads running along opposite sides of the optical device array.

FIG. 7B is a diagrammatic top view of a spacer substrate supporting a regular rectangular array of solderable bonding pads on opposite sides of an aperture.

DETAILED DESCRIPTION

In the following description, like reference numbers are used to identify like elements. Furthermore, the drawings are intended to illustrate major features of exemplary embodiments in a diagrammatic manner. The drawings are not intended to depict every feature of actual embodiments or relative dimensions of the depicted elements, and are not drawn to scale.

Referring to FIG. 1, each of the following embodiments may include one or more optical devices, including a vertical cavity surface emitting laser (VCSEL) 20 and a semiconductor diode. VCSEL 20 may be formed on a semiconductor substrate from alternating layers of semiconductor material. Each VCSEL includes a bottom mirror 22, a top mirror 24 and a gain region 26. Each VCSEL also may include one or more bonding pads (not shown) to which an electrical driving circuit of an adapter card may connect. In response to the application of an electrical current through the one or more bonding pads, VCSEL 20 may produce a laser beam 28 with a substantially circular cross-section and a well-controlled wavelength that is defined by the vertical distance separating bottom mirror 22 and top mirror 24. The surface dimension of the optical interface 30 of the VCSEL laser cavity typically is on the order of 10 μm .

As explained in detail below, the optical devices (e.g., VCSELs) of an optoelectronic device 10 may be passively aligned with an optical lens system by bonding metallization patterns of the optical device system and the optical lens system using solder bump reflow technology. This feature reduces manufacturing costs and manufacturing time. The sensitivity of optical device performance to the thickness of the optical device substrate also may be reduced by bonding the device side of the optical device substrate to the device bonding surface of the optical lens system. In addition, electrical connections may be made through the solder bump bonds, thereby avoiding the need for wirebond electrical connections. This feature reduces inductance and electromagnetic interference (EMI) emissions commonly associated with such wirebond connections.

Referring to FIG. 2, in one embodiment, optoelectronic device 10 includes an optical device system 40 having an optical device substrate 42 supporting an optical device 44 (e.g., a light detector, such as a p-i-n diode, or a light-emitter, such as a VCSEL) and a solderable metallization pattern 46, 48 having a spatial arrangement with respect to optical device 44. Optoelectronic device 10 also includes an optical lens system 50 having an optical element 52 and a device bonding surface 54 supporting a solderable metallization pattern 56, 58 with a spatial arrangement with respect to optical element 52. The metallization patterns 46, 48 and 56, 58 may match identically or they may be different, in either case, however, the metallization patterns 46, 48 and 56, 58 are arranged so that when they are solder bonded together optical device 44 and optical element 52 are aligned. Optical element 52 may include a device-side optical lens 60 and a fiber-side optical lens 62. Optical lenses 60, 62 may be diffractive or refractive optical lenses formed on an optical substrate 64 (e.g., a glass substrate). Optoelectronic device 10 further includes a plurality of solder bumps 66 disposed between the metallization patterns 46, 48 and 56, 58. During manufacture, solder bumps 66 originally are disposed on metallization pattern 56, 58 of optical lens system 50. Optical device substrate 42 is aligned with optical substrate 64 to within an accuracy required for solder bumps 66 to contact the metallization pattern 46, 48 of optical device system 40. The assembly then is raised to a temperature at or above the melting point of solder bumps 66. Solder bumps 66 wets the solderable metallization pattern 46, 48 and surface tension forces pull optical substrate 64 and optical device substrate 42 in very precise alignment (e.g., to within $\pm 4 \mu\text{m}$). The assembly is cooled to form a solidly bonded, accurately aligned structure. This bonded structure may be incorporated into a header block of a transceiver module and aligned with the optical fibers of fiber optic ribbon interconnect 14 using conventional ferrule-based alignment technology.

In the resulting structure of optoelectronic device 10, solder bump reflow between metallization patterns 46, 48 and 56, 58 accurately aligns optical lenses 60, 62 with optical device 44 in the X-Y plane (i.e., orthogonal to a Z-axis 68, which corresponds to the axis of light transmission between optical device system 40 and optical lens system 50). In addition, optical lenses 60, 62 and optical device 44 are aligned along Z-axis 68 to achieve a desired focal distance between

optical device 44 and optical element 52. In the embodiment of FIG. 2, the Z-axis alignment is achieved by adjusting the dimension 70 of solder bumps 66 along Z-axis 68. Dimension 70 may be controlled by balancing surface tension and gravitational forces at the bonding temperature based upon a number of parameters, including individual solder bump volumes, wettable pad sizes, substrate mass and solder surface tension.

As shown in FIG. 3, in another embodiment, Z-axis alignment between optical device 44 and optical element 52 may be achieved by recessing optical element 52 below device bonding surface 54 to separate optical device 44 from optical element 52 by a distance 72 needed to achieve a desired focal distance between optical device 44 and optical element 52. Optical element 52 may be recessed below device bonding surface using conventional lithography and etching techniques.

Referring to FIG. 4A, in another optoelectronic device embodiment, Z-axis alignment between optical device 44 and optical element 52 is achieved by disposing between optical substrate 64 and optical device substrate 42 a spacer substrate 80 that includes an aperture 82, which enables light to pass between optical device 44 and optical element 52. In this embodiment, device bonding surface 54 – which supports metallization pattern 56, 58 – defines one face of spacer substrate 80. The Z-axis thickness of spacer substrate 80 is selected to separate optical device 44 from optical element 52 by a distance 84 needed to achieve a desired focal distance between optical device 44 and optical element 52. Spacer substrate 80 may be formed from a semiconductor material, such as silicon, and aperture 82 may be formed using conventional lithography and etching techniques. Spacer substrate 80 may be bonded to optical substrate 64 by conventional wafer bonding processes (e.g., adhesive bonding, silicon fusion bonding, anodic bonding and thermo-compressive bonding processes). Wafer bonding processes advantageously enable optoelectronic devices 10 to be manufactured using batch processing techniques.

Referring to FIG. 4B, in an alternative optoelectronic device embodiment, spacer substrate 80 and optical substrate 64 may be bonded together using a flip-chip solder bonding process. In this embodiment, spacer substrate 80 includes a fiber-side metallization pattern 90, 92 and optical substrate 64 includes a

metallization pattern 94, 96. A plurality of solder bumps 98 are disposed between metallization patterns 90, 92 and 94, 96 to bond optical element 52 in alignment with aperture 82. The Z-axis thickness of spacer substrate 80 and the Z-axis dimension of solder bumps 98 are selected to separate optical device 44 from optical element 52 by a distance 100 needed to achieve a desired focal distance between optical device 44 and optical element 52. During manufacture, solder bumps 98 originally are disposed on metallization pattern 94, 96 of optical substrate 64. Optical substrate 64 is aligned with spacer substrate 80 to within an accuracy required for solder bumps 98 to contact the metallization pattern 90, 92 of spacer substrate 80. The assembly then is raised to a temperature at or above the melting point of solder bumps 98. Solder bumps 98 wet the solderable metallization pattern 90, 92 and surface tension forces pull optical substrate 64 and spacer substrate 80 into very precise alignment (e.g., to within $\pm 4 \mu\text{m}$). The assembly is cooled to form a solidly bonded, accurately aligned structure.

Referring to FIGS. 5A and 5B, optoelectronic device 10 may include one or more optical devices 44 and a corresponding number of optical elements 52. As shown in FIG. 5A, spacer substrate 80 may include a single aperture 110 through which light is transmitted between the pairs of optical devices 44 and optical elements 52. Alternatively, as shown in FIG. 5B, spacer substrate 80 may include an aperture 112, 114, 116 for each pair of optical devices 44 and optical elements 52.

As shown in FIGS. 6A and 6B, in some embodiments, an integrated circuit 120, which is configured to drive the optical devices of optical device system 40, may be formed integrally with spacer substrate 80 by conventional semiconductor processing techniques (FIG. 6A). Alternatively, integrated circuit 120 may be bonded to spacer substrate 80 by a conventional flip-chip solder bonding process (FIG. 6B).

In each of the above-described embodiments, the metallization patterns may be arranged in a variety of ways to achieve a range of alignment accuracies. For example, in one embodiment, the metallization pattern of optical device system 40 (and consequently the metallization pattern of device bonding surface 54) may consist of two staggered arrays 130, 132 of solderable bonding pads 134 running along opposite sides of a linear array of optical devices 44, as shown in

WHAT IS CLAIMED IS:

- 1 1. An optoelectronic device, comprising:
2 an optical device system comprising an optical device substrate supporting
3 one or more optical devices and a solderable metallization pattern having a spatial
4 arrangement with respect to the one or more optical devices;
5 an optical lens system comprising one or more optical lenses and a device
6 bonding surface supporting a solderable metallization pattern having a spatial
7 arrangement with respect to the one or more optical lenses; and
8 a plurality of solder bumps disposed between the metallization patterns of
9 the optical device system and the optical lens system;
10 wherein the plurality of solder bumps bond the optical device substrate to
11 the device bonding surface with the one or more optical devices aligned with the
12 one or more optical lenses.
- 1 2. The optoelectronic device of claim 1, wherein the one or more
2 optical lenses are incorporated into the device bonding surface.
- 1 3. The optoelectronic device of claim 1, wherein the one or more
2 optical lenses are recessed below the device bonding surface.
- 1 4. The optoelectronic device of claim 1, wherein the optical lens
2 system comprises an optical substrate incorporating the one or more lenses and
3 the device bonding surface defines one face of a spacer substrate.
- 1 5. The optoelectronic device of claim 4, wherein the optical substrate
2 is bonded to the spacer substrate by a wafer bonding process.
- 1 6. The optoelectronic device of claim 4, wherein the optical substrate
2 is bonded to the spacer substrate by a flip-chip solder bonding process.
- 1 7. The optoelectronic device of claim 4, wherein the thickness of the
2 spacer substrate is selected based upon a representative focal distance between
3 the one or more optical devices and the one or more optical lenses.

8. The optoelectronic device of claim 4, wherein the spacer substrate comprises one or more apertures through which light is transmitted between the one or more optical devices and the one or more optical lenses.

9. The optoelectronic device of claim 4, further comprising an integrated circuit formed on the spacer substrate and configured to drive the one or more optical devices.

10. The optoelectronic device of claim 4, further comprising an integrated circuit bonded to the spacer substrate by a flip-chip solder bonding process and configured to drive the one or more optical devices.

11. The optoelectronic device of claim 1, wherein a characteristic dimension of the plurality of solder bumps is selected based upon a representative focal distance between the one or more optical devices and the one or more optical lenses.

12. The optoelectronic device of claim 1, wherein the one or more optical devices comprises a vertical cavity surface emitting laser or a detector, or both.

13. An optoelectronic device, comprising:
an optical lens system comprising a lens substrate supporting one or more optical lenses, and a spacer substrate defining one or more apertures therethrough; and

an optical device system comprising a device substrate supporting one or more optical devices;

wherein the lens substrate is bonded to the spacer substrate and the spacer substrate is bonded to the device substrate with the one or more optical lenses, the one or more optical apertures and the one or more optical devices held together in registered alignment.

14. A method of aligning an optical device system and an optical lens system, comprising:

positioning an optical device system having one or more of optical devices and a solderable metallization pattern adjacent to an optical lens system having

5 one or more of optical lenses and a solderable metallization pattern with a
6 plurality of solder bumps disposed thereon; and
7 heating the plurality of solder bumps to a temperature at or above the
8 melting point of the solder bumps;
9 wherein, upon cooling, the plurality of solder bumps bond the optical
10 device system to the optical lens system with the one or more optical devices
11 aligned with the one or more optical lenses.

1 15. The method of claim 14, wherein the optical lens system comprises
2 an optical substrate incorporating the one or more lenses and a spacer substrate
3 supporting the metallization pattern of the optical lens system.

1 16. The method of claim 15, further comprising bonding the optical
2 substrate to the spacer substrate.

1 17. The method of claim 15, further comprising selecting the thickness
2 of the spacer substrate based upon a representative focal distance between the
3 one or more optical devices and the one or more optical lenses.

1 18. The method of claim 15, further comprising forming in the spacer
2 substrate one or more apertures through which light is transmitted between the
3 one or more optical devices and the one or more optical lenses.

1 19. The method of claim 15, further comprising processing the spacer
2 substrate to form an integrated circuit configured to drive the one or more optical
3 devices.

1 20. The method of claim 14, further comprising bonding an integrated
2 circuit configured to drive the one or more optical devices to the spacer substrate
3 by a flip-chip solder bonding process.

ALIGNING AN OPTICAL DEVICE SYSTEM WITH AN OPTICAL LENS SYSTEM

ABSTRACT

A scheme (systems and methods) for passively aligning one or more optical devices with a corresponding number of optical lenses in an accurate and efficient manner is described. By this approach, the invention avoids the often labor-intensive and costly steps required by conventional active alignment techniques that attempt to align the optical devices to the optical fibers. In one aspect, an optoelectronic device includes an optical device system, an optical lens system and a plurality of solder bumps disposed therebetween. The optical device system includes an optical device substrate supporting one or more optical devices and a solderable metallization pattern having a spatial arrangement with respect to the one or more optical devices. The optical lens system includes one or more optical lenses and a device bonding surface supporting a solderable metallization pattern having a spatial arrangement with respect to the one or more optical lenses. The solder bumps are disposed between the metallization patterns of the optical device system and the optical lens system. The plurality of solder bumps bond the optical device substrate to the device bonding surface with the one or more optical devices aligned with the one or more optical lenses. In another aspect, the optical lens system includes a spacer substrate defining one or more apertures therethrough. A method of aligning an optical device system and an optical lens system also is described.

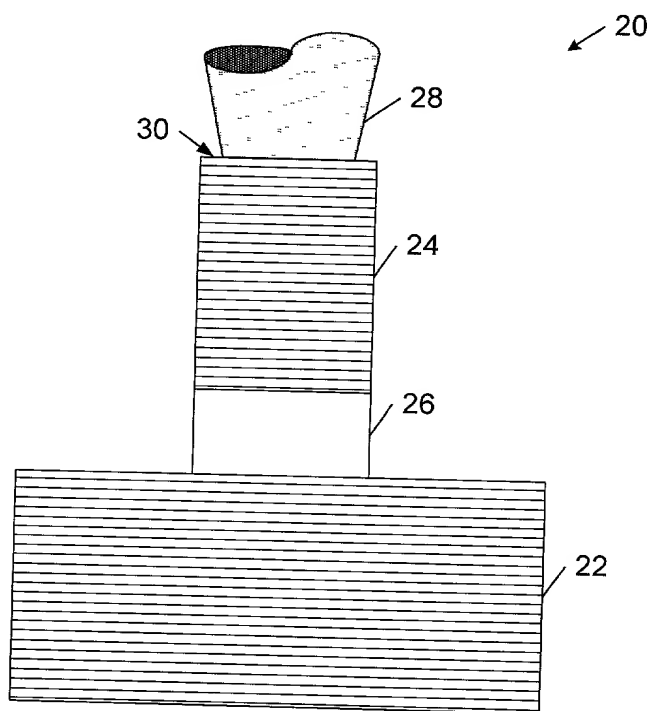


FIG. 1

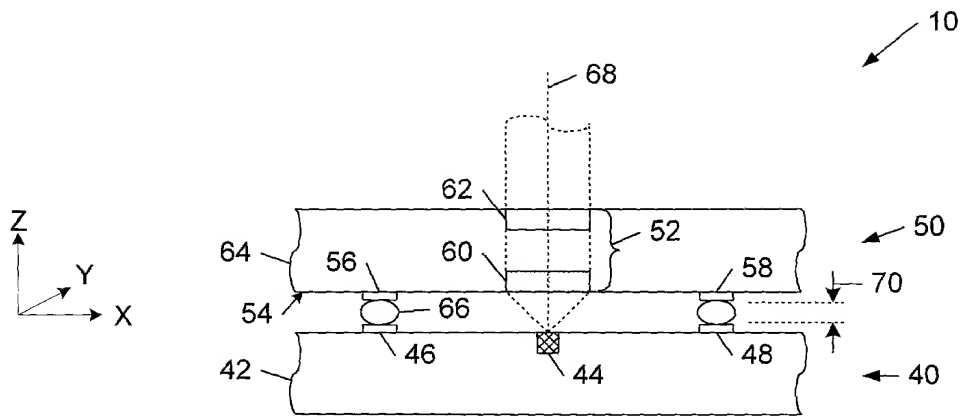


FIG. 2

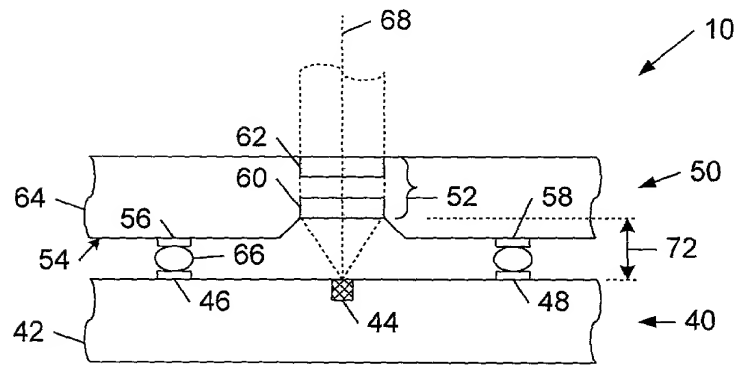
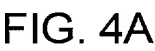
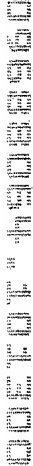
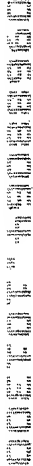


FIG. 3



[illegible][illegible]

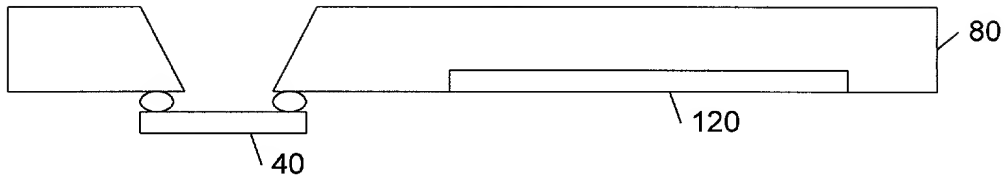


FIG. 6A

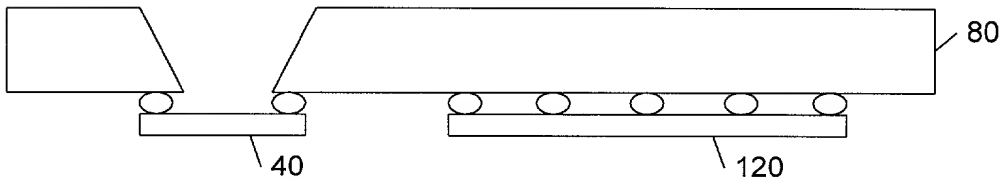


FIG. 6B

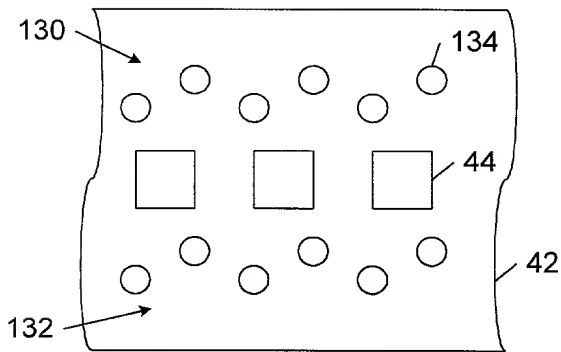


FIG. 7A

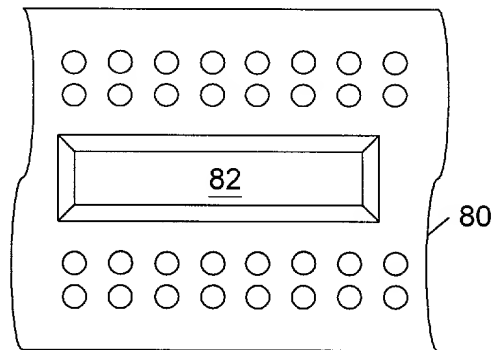


FIG. 7B

PATENT APPLICATION

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 10001197

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ALIGNING AN OPTICAL DEVICE SYSTEM WITH AN OPTICAL LENS SYSTEM

the specification of which is attached hereto unless the following box is checked:

() was filed on _____ as US Application Serial No. or PCT International Application
Number _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES NO.
			YES NO

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Customer Number 022878

Place Customer
Number Bar Code
Label hereSend Correspondence to:
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Legal Department, 51U-PD
Intellectual Property Administration
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

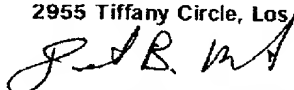
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Inventor's Signature



Date

9-7-2000

Rev 05/00 (DecPwr)

(Use Page Two For Additional Inventor(s) Signature(s))

Page 1 of 2

DOCKET "450222550"

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (continued)

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Inventor's Signature

Date

9/8/2000

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Inventor's Signature

Date

Full Name of # 4 joint inventor:

Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 5 joint inventor:

Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 6 joint inventor:

Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 7 joint inventor:

Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 8 joint inventor:

Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

DOCKET "4908360"

FOR PATENT APPLICATION (continued)

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Date _____

Citizenship: United States

Residence: 5705 Lois Lane, Edina, MN 55439

Post Office Address: 5705 Lois Lane, Edina, MN 55439

Inventor's Signature _____

Date _____

Full Name of # 4 joint inventor:

Citizenship:

Residence:

Post Office Address:

INVENTOR'S SIGNATURE

Date

Full Name of # 5 joint inventor:

Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date _____

Full Name of # 6 Joint inventor:

Citizenship:

Residence:**Post Office Address:**

INVENTOR'S SIGNATURE

Date _____

Full Name of # 7 joint inventor:

Citizenship:

Residence:

Post Office Address:

INVENTOR'S SIGNATURE

Date _____

Full Name of # 8 joint inventor:

Citizenship:

Residence:**Post Office Address:**

INVENTOR'S SIGNATURE

Date _____